SH-III/Physics-303C-7(T)/19

B.Sc. Semester III (Honours) Examination, 2018-19

PHYSICS

Course ID : 32413 **Course Code : SHPHS-303C-7(T)**

Course Title : Digital Systems and Applications

Time: 1 Hour 15 Minutes **Full Marks: 25**

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Section–I

1. Answer *any five* questions: 1×5=5

(a) Convert $(11101{\cdot}101)_2$ into decimal number.

(b) Prove that $\left(B\overline{C} + \overline{A}D\right)\left(A\overline{B} + C\overline{D}\right) = 0$.

(c) What is the limitation of half adder?

(d) How does a sequential logic system differ from combinational logic system?

(e) Write de Morgan's theorems.

(f) How many select inputs are required for 8 : 1 multiplexer?

(g) What is monolithic integrated circuit?

(h) What is 'Cache' memory?

Section–II

Answer *any two* questions: 5×2=10

2. What do you mean by positive logic? Draw the circuit diagram of positive logic AND and OR gates using diodes and explain their operations. 1+(2+2)=5

3. What is a multiplexer? Design a 4 : 1 multiplexer using basic gates and explain its operation with truth table. 1+4=5

4. Draw the functional block diagram of 555 timer. Explain the operation of an astable multivibrator using 555 timer. 1+4=5

5. Given $f = AB + AC + C + AD + ABC$, express f in standard SOP form. Minimize it using K-map. Realize the minimized expression using NAND gates only. 1+3+1=5

Section–III

Answer *any one* question: 10×1=10

6. (a) What is flip-flop? Write down some uses of flip-flops.

(b) Is there any difference between latch and Flip-flop?

(c) What is S-R flip-flop? Explain the operation of a clocked SR flip-flop with truth table.

(d) What do you mean by race around condition? (1+1)+1+(1+5)+1=10

7. (a) Discuss the principle of operation of a binary full adder circuit by drawing proper circuit diagram. Write the Boolean expressions of its 'Sum' and 'Carry' outputs.

(b) Draw the circuit diagram of a serial-in serial-out 4 bit shift register and explain its working principle. (4+2)+(2+2)=10

———————